REMARKS

Claims 1, 4-5, 7, 9-11, 14-15, and 23 are pending in the present application. Reconsideration and allowance of pending claims 1, 4-5, 7, 9-11, 14-15, and 23 in view of the following remarks are requested.

In the Office Action dated November 14, 2003, the Examiner has ***finally rejected*** claims 1, 4-5, 7, 9-11, 14-15, and 23 on the basis of new ground(s) of rejection. Applicant respectfully requests reconsideration and withdrawal of the finality of the rejection of the Office Action dated November 14, 2003.

The Examiner has rejected claims 1, 4-5, 7, 9-11, 14-15, and 23 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,808,339 to Yamagishi et al. ("Yamagishi") taken with "ULSI Technology," p. 211, by Sze et al. ("Sze") or U.S. patent number 4,613,956 to Paterson et al. ("Paterson") and in view of "Applicant's admitted prior art." For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, and 23, is patentably distinguishable over Yamagishi, Sze, and Patterson, singly or any combination thereof.

The present invention, as defined by independent claims 1, 7, and 23, teaches, among other things, depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. As disclosed in the patent application, an insulator layer

comprising a high quality oxide, such as LPCVD furnace grown oxide, is formed over a floating gate and directly on exposed portions of a tunnel oxide layer. Alternatively, as disclosed in the present application, the insulator can comprise other insulator materials, such as nitride and silicon oxide, if the floating gate undergoes a thermal oxidation process to form a sealing layer of oxide on the sides of the floating gate prior to formation of the insulator layer. Thus, as disclosed in the present application, by forming an insulator layer comprising a high quality oxide, such as LPCVD furnace grown oxide, over a floating gate or, alternatively, by forming a layer of thermal oxide on the sides of the floating gate prior to formation of the insulator layer, the present invention advantageously prevents charge from leaking out of the vertical side surfaces of the float gate.

Further, as disclosed in the present application, after the insulator layer has been deposited, the insulator layer is polished using chemical-mechanical polishing technique until a thickness of a second region of the insulator layer is substantially equal to a thickness of the floating gate. As a result, the present invention achieves a level, planar layer comprising the floating gate and the insulator layer, which advantageously provides a level surface on which an ONO layer and a control gate layer can be subsequently deposited.

In contrast to the present invention as defined by independent claims 1, 7, and 23, Yamagishi does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a

tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. Yamagishi specifically discloses electrode pattern 53 formed over first gate insulating layer 51 and second insulating layer 54 formed over electrode pattern 53 and element isolation region 13, where insulating layer 54 is formed by a CVD method. See, for example, column 12, lines 11-30 and Figures 9A-9E. In Yamagishi, first insulating layer 51 is formed on element formation region 12 of semiconductor substrate 11 by a heat oxidation method. See, for example, column 12, lines 11-14 and Figure 9C of Yamagishi.

However, Yamagishi does not teach, disclose, or suggest forming first gate insulating layer 51 over element isolation region 13, which is formed around element formation region 12. Thus, in Yamagishi, first gate insulating layer 51 is situated only under electrode pattern 53 and, consequently, not formed directly on first gate insulating layer 51 (i.e. a tunnel oxide layer) as specified in independent claims 1, 7, and 23. In Yamagishi, insulating layer 51 is formed by a CVD method, not an LPCVD process as specified in independent claims 1, 7, and 23. Thus, in Yamagishi, insulating layer 51 does not comprise LPCVD furnace grown oxide, which is a high quality oxide that prevents charge from leaking out of the vertical side surfaces of the floating gate. Moreover, Yamagishi fails to teach, disclose, or suggest insulating layer 51 comprising a high quality oxide such that insulating layer 51 prevents charge form leaking out of the

vertical side surfaces of the floating gate. Additionally, Yamagishi does not provide a motivation for forming an insulating layer comprising LPCVD furnace grown oxide.

In contrast to the present invention as defined by independent claims 1, 7, and 23, Sze does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process. Sze is cited by the Examiner to disclose the advantages provided by a dielectric layer formed by using a LPCVD process. However, Sze does not teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process. Furthermore, Sze does not teach, disclose, or suggest utilizing an insulator formed by a LPCVD process and covering the sides of a floating gate such that the LPCVD-formed insulator prevents charge from leaking out of the sides of the floating gate. Thus, Sze fails to overcome the deficiencies of Yamagishi discussed above.

In contrast to the present invention as defined by independent claims 1, 7, and 23, Paterson does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality

oxide (claim 23) is formed by a LPCVD process. Paterson specifically discloses depositing an LPCVD dielectric on a floating gate in order to provide high uniformity. See, for example, Paterson, column 3, lines 54-68. However, Paterson does not teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer is formed by a LPCVD process. Furthermore, Paterson does not teach, disclose, or suggest utilizing an insulator formed by a LPCVD process and covering the sides of a floating gate such that the LPCVD-formed insulator prevents charge from leaking out of the sides of the floating gate. Thus, Paterson fails to overcome the deficiencies of Yamagishi discussed above.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, and 23, is not suggested, disclosed, or taught by Yamagishi, Sze, and Paterson, singly or in any combination thereof. As such, the present invention, as defined by independent claims 1, 7, and 23, is patentably distinguishable over Yamagishi, Sze, and Paterson. Thus claims 4-5 depending from independent claim 1 and claims 9-11 and 14-15 depending from independent claim 7, are, *a fortiori*, also patentably distinguishable over Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 1, 4-5, 7, 9-11, and 23 under 35 USC §103(a) as being unpatentable over U.S. patent number 6,033,956 to Shye-Lin Wu

("Wu") or U.S. patent number 4,713,142 to Mitchell et al. ("Mitchell") taken with Yamagishi, and in view of Sze or Paterson. For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, and 23, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson, singly or any combination thereof.

In contrast to the present invention as defined by independent claims 1, 7, and 23, Wu does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer." Wu specifically discloses depositing CVD TEOS oxide 210 over polysilicon layer 204 and polysilicon slots 205, spinning planarizing photoresist 212 on the wafer, applying a second resist coat, and utilizing a planarizing plasma etch to etch both CVD TEOS oxide layer 210 and photoresist 212 such that the surface of polysilicon layer 204 is exposed. See, for example, Wu, column 1, lines 46-58.

However, Wu fails to teach, disclose, or suggest an insulating layer comprising a high temperature oxide or a high quality oxide that is formed by an LPVCD process. Moreover, Wu fails to teach, disclose, or suggest CVD TEOS oxide layer 210 comprising

a high quality oxide such that CVD TEOS oxide layer 210 prevents charge form leaking out of the vertical side surfaces of a floating gate. Additionally, Wu does not provide a motivation for forming an insulating layer comprising LPCVD furnace grown oxide.

Furthermore, Wu fails to teach, disclose, or suggest polishing the insulator layer immediately after insulator layer has been deposited. In Wu, after CVD TEOS oxide layer 210 is deposited, two photoresist coats are applied and a planarizing plasma etch is utilized to etch both CVD TEOS oxide layer 210 and photoresist 212.

In contrast to the present invention as defined by independent claims 1, 7, and 23, Mitchel does not teach, disclose, or suggest depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process, and "polishing the insulator layer immediately after the step of depositing the insulator layer to reduce the thickness of the insulator layer and to provide a planar surface that exposes a top surface of the floating gate and the insulator layer." Mitchel specifically discloses subjecting polycrystalline silicon layer 33 and gate oxide layer 32, which are formed on the surface of substrate 1, and subjecting polycrystalline silicon layer 33 to a thermal oxidation to form silicon dioxide layer 36. See, for example, column 2, lines 64-68, column 3, line 1, and Figure 2b of Mitchel. In Mitchel, silicon dioxide layer 37 is then formed by chemical vapor deposition on silicon dioxide layer 36, photoresist layer 38 is formed over silicon dioxide

layer 37, and an anisotropic etching process is utilized to etch photoresist layer 38 and silicon dioxide layer 37. See, for example, column 3, lines 8-19 and Figures 2c and 2d of Mitchel. Thus, in Mitchel, silicon dioxide layer 36 is situated between silicon dioxide layer 37 and polycrystalline silicon layer 33 and gate oxide layer 32. The Examiner states that both silicon dioxide layer 36 and silicon dioxide layer 37 can be considered as an insulating layer. See, for example, page 6, first paragraph of the Office Action dated November 14, 2003.

However, silicon dioxide layer 36 is formed by thermal oxidation and silicon dioxide layer 37 is formed by a CVD process. Thus, silicon dioxide layer 36 and silicon dioxide layer 37 are two distinct layers that are formed by completely different processes. Thus, Mitchel fails to teach, disclose, or suggest depositing an insulator layer directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, where the insulator layer is deposited to a thickness greater than the thickness of the floating gate. Additionally, Mitchell fails to teach, disclose, or suggest an insulator layer formed in a LPCVD process as specified in independent claims 1, 7, and 23. Furthermore, in Mitchell, photoresist layer 38 is formed over silicon dioxide layer 37 before an etch process is performed to expose the surface of polysilicon layer 33. Thus, Mitchell fails to teach, disclose, or suggest polishing the insulator layer immediately after the insulator layer has been deposited.

As discussed above, in contrast to the present invention as defined by independent claims 1, 7, and 23, Yamagishi, Sze, and Paterson do not teach, disclose, or suggest

depositing an insulator layer comprising a high temperature oxide (claims 1 and 7) or high quality oxide (claim 23) directly on a tunnel oxide layer and a floating gate, where the insulator layer is in contact with vertical surfaces of the floating gate, and where the insulator layer (claims 1 and 7) or high quality oxide (claim 23) is formed by a LPCVD process.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 1, 7, and 23, is not suggested, disclosed, or taught by Wu, Mitchell, Yamagishi, Sze, and Paterson, singly or any combination thereof. As such, the present invention, as defined by independent claims 1, 7, and 23, is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson. Thus claims 4-5 depending from independent claim 1 and claims 9-11 depending from independent claim 7, are, *a fortiori*, also patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The Examiner has further rejected claims 14-15 under 35 USC §103(a) as being unpatentable over Wu or Mitchell taken with Yamagishi and in view of Sze or Paterson as applied to claims 1, 4-5, 7, 9-11, and 23, and further in view of "Applicant's admitted prior art." As discussed above, independent claim 7 is patentably distinguishable over Wu, Mitchell, Yamagishi, Sze, and Paterson and, as such, claims 14-15 depending from independent claim 7 are, *a fortiori*, also patentably distinguishable over Wu, Mitchell,

Yamagishi, Sze, and Paterson for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by independent claims 1, 7, and 23 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1, 4-5, 7, 9-11, 14-15, and 23 pending in the present application is respectfully requested.

Respectfully Submitted,
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Date: Feb. 3, 2004

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